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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,308	01/21/2004	Rolf Nuchter	Q79383	9883
23373	7590	06/09/2009	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER			
		2416		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/760,308	<b>Applicant(s)</b> NUCHTER, ROLF
	<b>Examiner</b> JEFFREY M. RUTKOWSKI	<b>Art Unit</b> 2416

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 26 February 2009.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-9, 11, 12 and 16-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-9, 11-12 and 16-19 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/06)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

## **DETAILED ACTION**

**Claims 10, 13-15** have been cancelled.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
3. **Claims 1-9, 11-12 and 16-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Afrashteh et al. (US Pat 5,426,641), hereinafter referred to as Afrashteh in view of Hirvilampi (US Pat 6,351,189).
4. For **claims 1, 7-8, 11-12 and 16-19**, Afrashteh teaches a power amplifier is made up of a high gain transistor (MESFET), a resistor 211 (shunt) connected in series with a drain circuit 205 and a microprocessor 210 (controlling unit) [col. 15 lines 30-35, col. 16 lines 4-6 and figure 2]. Figure 3 shows each step is performed at different null timeslots.
5. Afrashteh teaches the microprocessor performs deviation detection. The adjustment of the bias is performed by the gate bias control unit 204 [col. 16 lines 10-28], not the

microprocessor. Domino teaches the adjustment of bias by a controlling unit limitation absent from the teachings of Afrashteh by disclosing a DSP chip that processes data and adjusts a bias value [col. 7 lines 7-12, 25-30 and figure 1]. It would have been obvious to a person of ordinary skill in the art at the time of the invention use a DSP chip in Afrashteh's invention since DSP chips are more powerful than general-purpose microprocessors via being more application specific.

6. Afrashteh does not disclose detecting an occurrence of null timeslots. Hirvilampi discloses a bias control circuit that uses a switching device that detects null timeslots by switching to a bias control circuit when an amplifier is not transmitting [col. 6 lines 59-63]. Hirvilampi's invention bias adjustments are performed when the amplifier is not transmitting (null timeslots), including two separate null timeslots [col. 6 lines 54-56]. Since information can only be transmitted in only one of eight time slots [col. 4 lines 25-30], Hirvilampi suggests that two null timeslots could occur before and after a data slot. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Hirvilampi's bias adjustment mechanism in Afrashteh's invention to provide for the auto-biasing of an amplifier [**Hirvilampi, title**].

7. Specifically for **claims 7-8 and 18-19**, Afrashteh suggests waiting until a transistor has reached a steady state temperature to start controlling the by disclosing the bias adjustment does not start until a few timeslots (at least three null timeslots) after the transmission timeslot [**figure 3**].

8. Specifically for **claims 16 and 17**, Afrashteh does not disclose where null power timeslots occur. According to Hirvilampi, information can only be transmitted in only one of

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eight time slots [col. 4 lines 25-30], suggesting that a null power timeslot can occur before a data timeslot and another null power timeslot occurs after the data timeslot. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Hirvilampi's timeslot assignment in Afrashteh's invention to provide time for the auto-biasing of an amplifier [Hirvilampi, title].

9. For claim 2, Afrashteh discloses checking and adjusting the bias at another null power time slot [col. 15 lines 53-60].

10. For claim 3, Afrashteh does not disclose the consecutive occurrence of null timeslots. Hirvilampi discloses information can only be transmitted in only one of eight time slots [col. 4 lines 25-30], which suggests null timeslots occur consecutively. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Hirvilampi's consecutive null timeslots to perform bias adjustment in Afrashteh's invention to provide time for the auto-biasing of an amplifier [Hirvilampi, title].

11. For claim 4, Afrashteh does not teach the use of control loops. Hirvilampi teaches the control loop limitation absent from the teachings of Afrashteh by disclosing an auto-bias system that uses a feedback loop (control loop) to adjust the bias of an amplifier between transmission periods (null timeslots) [abstract]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a control loop in Afrashteh's invention to ensure a signal is properly amplified [Hirvilampi, col. 5 lines 5-10].

12. For claim 5, Afrashteh discloses changes in temperature require the bias point to be readjusted [col. 14 line 66 to col. 15 line 3].

13. For **claim 6**, Afrashteh discloses the bias is the gate voltage of an amplifier [**col. 16 line 20**].

14. For **claim 9**, the combination of Afrashteh and Hirvilampi discloses a microprocessor **210**, which has a computer program stored thereon, for performing the **claim 1** method steps [**Afrashteh, col. 16 lines 5-10**].

15. Applicant's arguments filed 02/26/2009 have been fully considered but they are not persuasive, for the reasons stated above.

*Response to Arguments*

16. The arguments with respect to the prior art not disclosing each of the three operations is performed at a different timeslot is not persuasive because the claims do not require less than three operations to be performed in each null timeslot. The claims require each of the detection steps and the adjustment steps to be performed in different null time slots. However, the claims do not exclude each of the steps from being performed together in a single null time slot.

17. The Examiner would agree with the Applicant if the claims were to require that not all operations were performed in a single null time slot. For example, if the claims required no more than two or only one of the detecting the deviation, the detecting the occurrence, and the adjusting the bias is performed at each different null power time slots of the TDMA signal. The support is found at page 6 last paragraph, which was also cited by the Applicant.

18. The arguments with respect to the prior art not suggesting waiting until a transistor has reached a steady state temperature are not persuasive. Afrashteh's invention controls the sensitivity of the amplifier within a certain temperature range (see col. 15 lines 40-45). Also, the amplifier remains "on" after transmission while the measurements are taken (see col. 15 lines 55-

60). Figure 3 shows the three null timeslots have occurred because there is at least three null timeslots between start adjustments.

19. The arguments with respect to Hirvilampi not disclosing three operations performed are not persuasive because it is based on piecemeal analysis. For example, two operations were cited as being taught by Afrashteh.

***Conclusion***

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski  
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06/03/2009

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